Rev 6; 8/08

1024-Bit, 1-Wire EEPROM

DS2431

General Description

The DS2431 is a 1024-bit, 1-Wire® EEPROM chip organized as four memory pages of 256 bits each. Data is written to an 8-byte scratchpad, verified, and then copied to the EEPROM memory. As a special feature, the four memory pages can individually be write protected or put in EPROM-emulation mode, where bits can only be changed from a 1 to a 0 state. The DS2431 communicates over the single-conductor 1-Wire bus. The communication follows the standard 1-Wire protocol. Each device has its own unalterable and unique 64-bit ROM registration number that is factory lasered into the chip. The registration number is used to address the device in a multidrop, 1-Wire net environment.

Applications

Accessory/PCB Identification

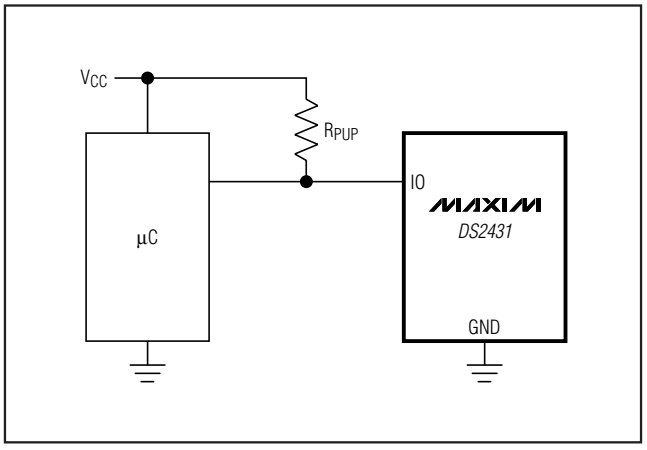
Medical Sensor Calibration Data Storage

Analog Sensor Calibration Including IEEE P1451.4 Smart Sensors

Ink and Toner Print Cartridge Identification

After-Market Management of Consumables

Typical Operating Circuit



Features

- **1024 Bits of EEPROM Memory Partitioned Into Four Pages of 256 Bits**
- **Individual Memory Pages Can Be Permanently Write Protected or Put in EPROM-Emulation Mode (“Write to 0”)**
- **Switchpoint Hysteresis and Filtering to Optimize Performance in the Presence of Noise**
- **IEC 1000-4-2 Level 4 ESD Protection (8kV Contact, 15kV Air, Typical)**
- **Reads and Writes Over a Wide Voltage Range from 2.8V to 5.25V from -40°C to +85°C**
- **Communicates to Host with a Single Digital Signal at 15.4kbps or 125kbps Using 1-Wire Protocol**
- **Also Available as Automotive Version Meeting AEC-Q100 Grade 1 Qualification Requirements (DS2431-A1)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2431+	-40°C to +85°C	3 TO-92
DS2431+T&R	-40°C to +85°C	3 TO-92
DS2431P+	-40°C to +85°C	6 TSOC
DS2431P+T&R	-40°C to +85°C	6 TSOC
DS2431G+	-40°C to +85°C	2 SFN
DS2431G+T&R	-40°C to +85°C	2 SFN
DS2431Q+T&R	-40°C to +85°C	6 TDFN-EP* (2.5k pcs)
DS2431X+S	-40°C to +85°C	3x3 UCSPR** (2.5k pcs)
DS2431X+	-40°C to +85°C	3x3 UCSPR** (10k pcs)

Note: *The leads of TO-92 packages on tape and reel are formed to approximately 100-mil (2.54mm) spacing. For details, refer to the package outline drawing.*
+ Denotes a lead-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*
***Contact factory for availability and guidelines on qualified usage conditions of the lead-free UCSPR.*

Pin Configurations appear at end of data sheet.

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1024-Bit, 1-Wire EEPROM

ABSOLUTE MAXIMUM RATINGS

IO Voltage Range to GND .....-0.5V to +6V
IO Sink Current 20mA
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature.....Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	(Note 2)	2.8		5.25	V
1-Wire Pullup Resistance	R_{PUP}	(Notes 2, 3)	0.3		2.2	kΩ
Input Capacitance	C_{IO}	(Notes 4, 5)			1000	pF
Input Load Current	I_L	IO pin at V_{PUP}	0.05		6.7	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 5, 6, 7)	0.5		V_{PUP} - 1.8	V
Input Low Voltage	V_{IL}	(Notes 2, 8)			0.5	V
Low-to-High Switching Threshold	V_{TH}	(Notes 5, 6, 9)	1.0		V_{PUP} - 1.0	V
Switching Hysteresis	V_{HY}	(Notes 5, 6, 10)	0.21		1.70	V
Output Low Voltage	V_{OL}	At 4mA (Note 11)			0.4	V
Recovery Time (Notes 2,12)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-Off Time (Notes 5, 13)	t_{REH}	Standard speed	0.5		5.0	µs
		Overdrive speed	Not applicable (0)			
Time Slot Duration (Notes 2, 14)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed	8			
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time (Note 2)	t_{RSTL}	Standard speed	480		640	µs
		Overdrive speed	48		80	
Presence-Detect High Time	t_{PDH}	Standard speed	15		60	µs
		Overdrive speed	2		6	
Presence-Detect Low Time	t_{PDL}	Standard speed	60		240	µs
		Overdrive speed	8		24	
Presence-Detect Sample Time (Notes 2, 15)	t_{MSP}	Standard speed	60		75	µs
		Overdrive speed	6		10	

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (Notes 2, 16, 17)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed, V_{PUP} > 4.5V	5		**15.5**	
		Overdrive speed	6		**15.5**	
Write-One Low Time (Notes 2, 17)	t_{W1L}	Standard speed	1		15	µs
		Overdrive speed	1		2	
IO PIN: 1-Wire READ						
Read Low Time (Notes 2, 18)	t_{RL}	Standard speed	5		15 - δ	µs
		Overdrive speed	1		2 - δ	
Read Sample Time (Notes 2, 18)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL} + δ		2	
EEPROM						
Programming Current	I_{PROG}	(Notes 5, 19)			0.8	mA
Programming Time	t_{PROG}	(Notes 20, 21)			10	ms
Write/Erase Cycles (Endurance) (Notes 22, 23)	N_{CY}	At +25°C	200k			—
		At +85°C (worst case)	50k			
Data Retention (Notes 24, 25, 26)	t_{DR}	At +85°C (worst case)	40			Years

Note 1: Specifications at T_A = -40°C are guaranteed by design only and not production tested.
Note 2: System requirement.
Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2482-x00, DS2480B, or DS2490 may be required.
Note 4: Maximum value represents the internal parasite capacitance when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied, the parasite capacitance does not affect normal communications.
Note 5: Guaranteed by design, characterization, and/or simulation only. Not production tested.
Note 6: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.
Note 7: Voltage below which, during a falling edge on IO, a logic 0 is detected.
Note 8: The voltage on IO must be less than or equal to V_{ILMAX} at all times the master is driving IO to a logic 0 level.
Note 9: Voltage above which, during a rising edge on IO, a logic 1 is detected.
Note 10: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic 0.
Note 11: The I-V characteristic is linear for voltages less than 1V.
Note 12: Applies to a single device attached to a 1-Wire line.
Note 13: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been reached on the preceding rising edge.
Note 14: Defines maximum possible bit rate. Equal to t_{W0LMIN} + t_{RECMIN}.
Note 15: Interval after t_{RSTL} during which a bus master is guaranteed to sample a logic 0 on IO if there is a DS2431 present. Minimum limit is t_{PDHMAX}; maximum limit is t_{PDHMIN} + t_{PDLMIN}.
Note 16: Numbers in **bold** are **not** in compliance with legacy 1-Wire product standards. See the *Comparison Table*.
Note 17: ε in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the master to pull the line low is t_{W1LMAX} + t_F - ε and t_{W0LMAX} + t_F - ε, respectively.
Note 18: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is t_{RLMAX} + t_F.

Note 19: Current drawn from IO during the EEPROM programming interval. The pullup circuit on IO during the programming interval should be such that the voltage at IO is greater than or equal to V_{PUPMIN}. If V_{PUP} in the system is close to V_{PUPMIN}, a low-impedance bypass of R_{PUP}, which can be activated during programming, may need to be added.

Note 20: Interval begins t_{REHMAX} after the trailing rising edge on IO for the last time slot of the E/S byte for a valid Copy Scratchpad sequence. Interval ends once the device's self-timed EEPROM programming cycle is complete and the current drawn by the device has returned from I_{PROG} to I_L.

Note 21: t_{PROG} for units branded version "A1" is 12.5ms. t_{PROG} for units branded version "A2" and later is 10ms.

Note 22: Write-cycle endurance is degraded as T_A increases.

Note 23: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 24: Data retention is degraded as T_A increases.

Note 25: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.

Note 26: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended; the device can lose its write capability after 10 years at +125°C or 40 years at +85°C.

COMPARISON TABLE

PARAMETER	LEGACY VALUES				DS2431 VALUES			
	STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)		STANDARD SPEED (µs)		OVERDRIVE SPEED (µs)	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (including t_{REC})	61	(undefined)	7	(undefined)	65*	(undefined)	8*	(undefined)
t_{RSTL}	480	(undefined)	48	80	480	640	48	80
t_{PDH}	15	60	2	6	15	60	2	6
t_{PDL}	60	240	8	24	60	240	8	24
t_{W0L}	60	120	6	16	60	120	6	**15.5**

**Intentional change; longer recovery time requirement due to modified 1-Wire front-end.*

***Note:** Numbers in **bold** are **not** in compliance with legacy 1-Wire product standards.*